AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Canceled).

2. (Currently amended) A frequency synthesizer, comprising:

a digitally controlled oscillator, including a plurality of switched capacitors;

control circuitry for selectively enabling and disabling said capacitors responsive to an oscillator tuning word, comprising:

select circuitry for enabling a number of capacitors responsive to said oscillator tuning word;

circuitry for dynamically varying which capacitors are enabled for a given oscillator tuning word to reduce non-linearities caused by slight variances in capacitive values; and ~~The frequency synthesizer of claim 1 wherein said control circuitry further includes~~ a switch matrix coupled to said select circuitry, said dynamically varying circuitry and said plurality of switched capacitors, said switch matrix having a plurality of switches selectively enabled by said select circuitry and said dynamically varying circuitry, said switches for enabling or disabling respective switched capacitors.

3. (Original) The frequency synthesizer of claim 2 and further comprising drivers coupled between said switches and respective capacitors.

4. (Original) The frequency synthesizer of claim 3 wherein said drivers comprise resampling drivers.

5. (Original) The frequency synthesizer of claim 2 wherein said switches are arranged in a plurality of predefined groups.

6. (Original) The frequency synthesizer of claim 5 wherein said dynamically varying circuitry varies a set of switches enabled in a group.

7. (Original) The frequency synthesizer of claim 6 wherein said dynamically varying circuitry rotates said set of switches within a group.

8. (Original) The frequency synthesizer of claim 5 wherein said dynamically varying circuitry varies a set of switches enabled in a plurality of groups.

9. (Original) The frequency synthesizer of claim 8 wherein said dynamically varying circuitry rotates said set of switches within a plurality of groups.

10. (Canceled).

11. (Currently amended) A method of synthesizing a frequency, comprising the steps of:

selectively enabling and disabling capacitors in a digitally controlled oscillator responsive to an oscillator tuning word;

circuitry for dynamically varying which capacitors are enabled for a given error signal value to reduce non-linearities caused by slight variances in capacitive values; and

~~The method of claim 10~~ wherein said selectively enabling step comprises the step of selectively enabling and disabling switches in a switch matrix responsive to said oscillator tuning word and said dynamically varying step comprises the step of dynamically varying which switches are enabled for a given error signal value.

12. (Original) The method of claim 11 wherein said switches are arranged in a plurality of groups.

13. (Original) The method of claim 12 wherein said dynamically varying step comprises the step of dynamically varying a set of switches enabled in a group.

14. (Original) The method of claim 13 wherein said dynamically varying step comprises the step of rotating said set of switches within a group.

15. (Original) The method of claim 12 wherein said dynamically varying step varies a set of switches enabled in a plurality of groups.

16. (Original) The method of claim 15 wherein said dynamically varying step rotates said set of switches within said plurality of groups.

17. (Original) A frequency synthesizer comprising:

a digitally controlled oscillator, including a plurality of switched capacitors; and

control circuitry for selectively enabling and disabling said capacitors, comprising:

circuitry for tuning said digitally controlled oscillator to a selected frequency by enabling and disabling capacitors in a first set; and

circuitry for modulating said digitally controlled oscillator by enabling and disabling capacitors in a second set.

18. (Original) The frequency synthesizer of claim 17 wherein said tuning circuitry comprises circuitry for initially enabling and disabling said capacitors in said first set responsive to a oscillator tuning word while leaving said second set of capacitors in a predetermined state.

19. (Original) The frequency synthesizer of claim 17 wherein said tuning circuitry comprises circuitry for enabling and disabling said capacitors in said first set and said second set responsive to a oscillator tuning word and, after obtaining said selected frequency, rearranging the enabled and disabled capacitors such that the second set of capacitors is in a predetermined state.

20. (Original) A method of synthesizing a frequency, comprising the steps of:

tuning a digitally controlled oscillator by enabling and disabling a first set of switched capacitors to reach a selected frequency; and

modulating said digitally controlled oscillator by enabling and disabling a second set of switched capacitors.

21. (Original) The method of claim 20 wherein said tuning step comprises the step of initially enabling and disabling said capacitors in said first set responsive to a oscillator tuning word while leaving said second set of capacitors in a predetermined state.

22. (Original) The method of claim 20 wherein said tuning step comprises the step of enabling and disabling said capacitors in said first set and said second set responsive to a oscillator tuning word and, after obtaining said selected frequency, rearranging the enabled and disabled capacitors such that the second set of capacitors is in a predetermined state.

23. (Original) A frequency synthesizer comprising:

a digitally controlled oscillator, including a first set of switched capacitors and a second set of switched capacitors, where said second set of switched capacitors are in a physically separate area from said first set of switched capacitors;

control circuitry for selectively enabling and disabling said capacitors responsive to an oscillator tuning word, comprising:

first tracking circuitry for enabling and disabling capacitors responsive to an first portion of said oscillator tuning word and a first clock;

second tracking circuitry for enabling and disabling capacitors responsive to a second portion of said oscillator tuning word and a second clock, wherein said second clock is significantly faster than said first clock.

24. (Original) The frequency synthesizer of claim 23, wherein said second tracking circuitry includes a digital dithering circuit.

25. (Original) The frequency synthesizer of claim 24, wherein said digital dithering circuit comprises a sigma-delta modulation circuit.

26. (Original) The frequency synthesizer of claim 23, wherein said first tracking circuitry enables and disables capacitors in said first set responsive to an integer portion of said oscillator tuning word and said second tracking circuitry enables and disables capacitors in said second set responsive to an fractional portion of said oscillator tuning word.

27. (Original) A method of synthesizing a frequency comprising the steps of:

enabling and disabling a first set of switched capacitors in a digitally controlled oscillator responsive to an first portion of an oscillator tuning word and a first clock;

enabling and disabling a second set of switched capacitors, physically separate from said first set, in the digitally controlled oscillator responsive to a second portion of an oscillator tuning word and a second clock, wherein said second clock is significantly faster than said first clock.

28. (Original) The method of claim 27, wherein said step of enabling and disabling said second set of capacitors comprises the step of modulating said second set with a digital dithering circuit.

29. (Original) The method of claim 28 wherein said modulating step comprises the step of modulating the second set using sigma-delta modulation.

30. (Original) The method of claim 27, wherein said step of enabling and disabling said first set of capacitors comprises the step of enabling and disabling said first set of capacitors responsive to an integer portion of said oscillator tuning word and said step of enabling and disabling said second set of capacitors comprises the step of enabling and disabling said second set of capacitors responsive to an fractional portion of said oscillator tuning word.